CMOS OPEN ENDED

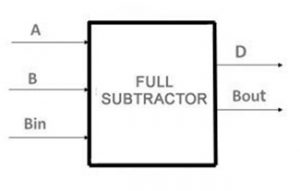
Full Subtractor

**Team 10**

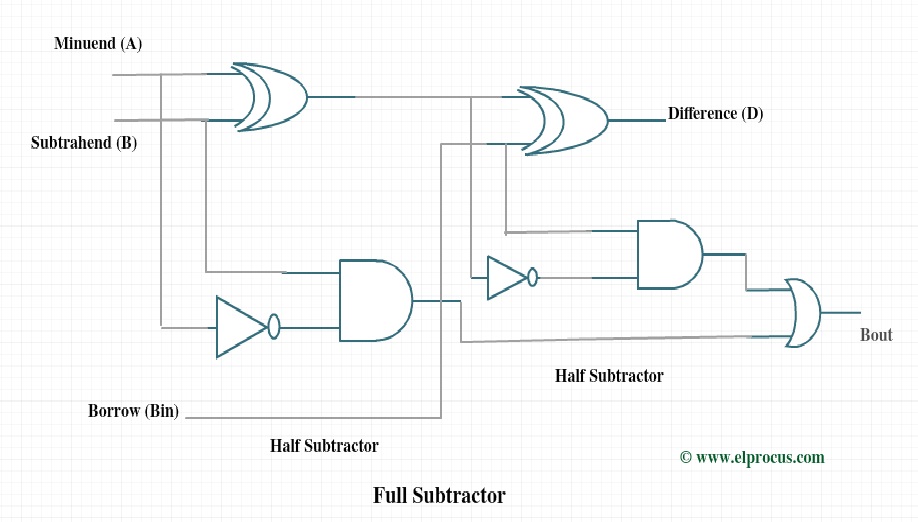
|  |  |
| --- | --- |
| Name | Roll No |
| Rohit Waddar | 308 |
| Gangadharayya.S.K | 314 |
| U K Samarth | 319 |

**Introduction:**

A full subtractor is a combinational circuit that performs subtraction of two bits, one is minuend and other is subtrahend, taking into account borrow of the previous adjacent lower minuend bit. This circuit has three inputs and two outputs. The three inputs A, B and Bin, denote the minuend, subtrahend, and previous borrow, respectively. The two outputs, D and Bout represent the difference and output borrow, respectively.



**Circuit Diagram:**



**Truth Table:**

Inputs Outputs

(A) (B) (Bin) (D) (Bout)

---------------------------------------------

0 0 0 0 0

0 0 1 1 1

0 1 0 1 1

0 1 1 0 1

1 0 0 1 0

1 0 1 0 0

1 1 0 0 0

1 1 1 1 1

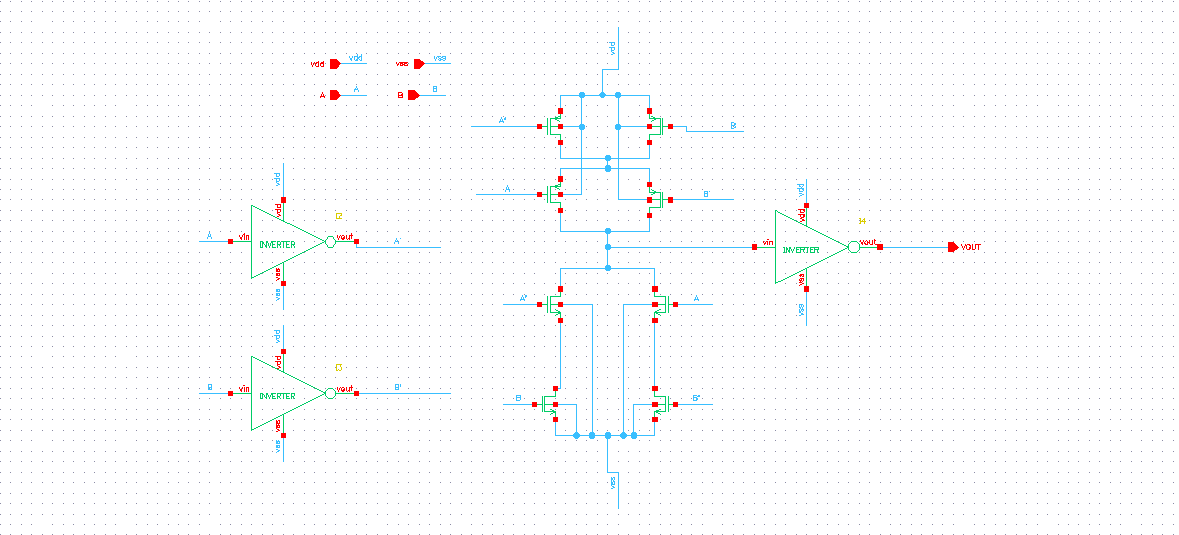
The expression for Difference is,

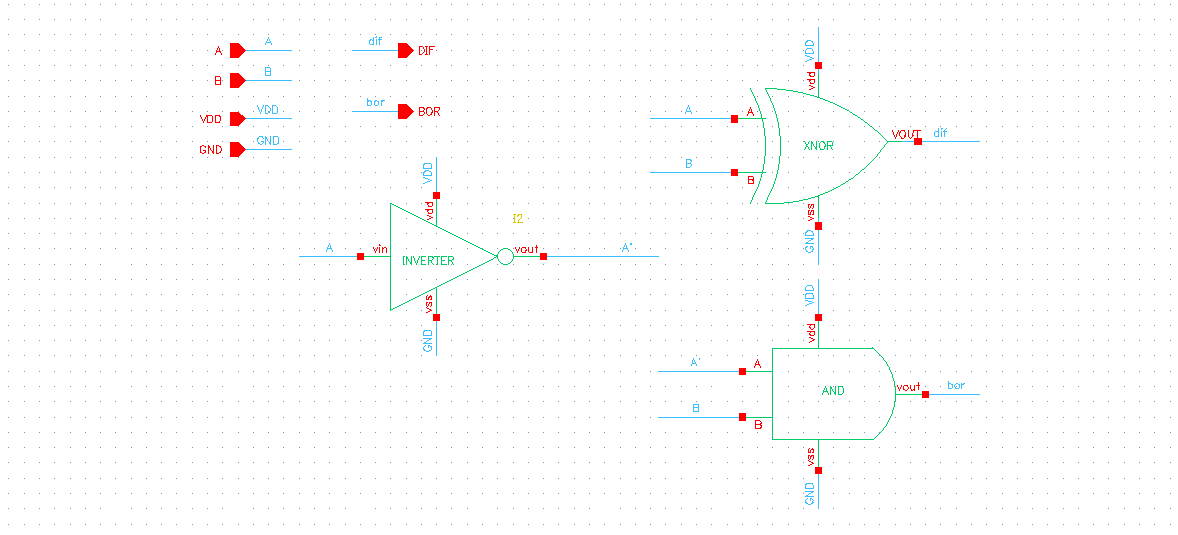
**D = A’B’Bin + AB’Bin’+ A’BBin’ + ABBin**

The expression for Borrow is,

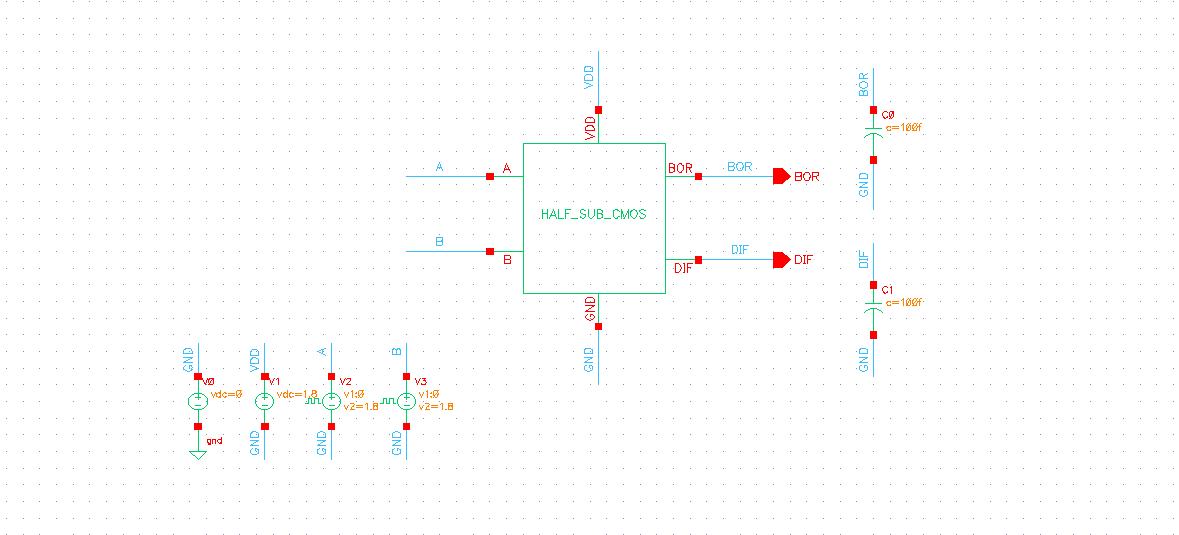
**Bout = A’Bin + A’B + BBin**

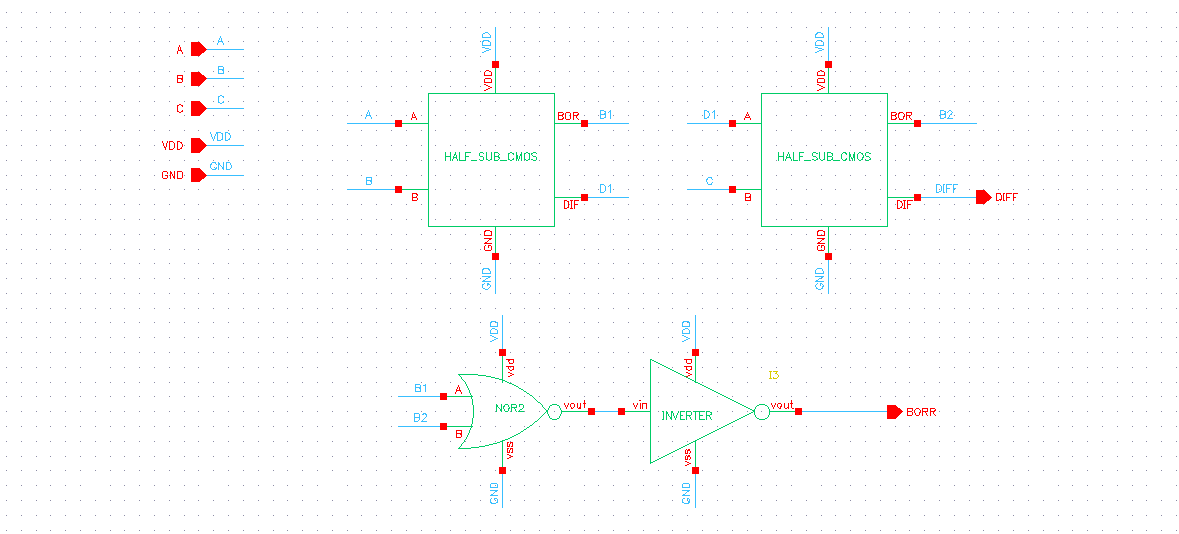
**XOR schematic CMOS Logic:**

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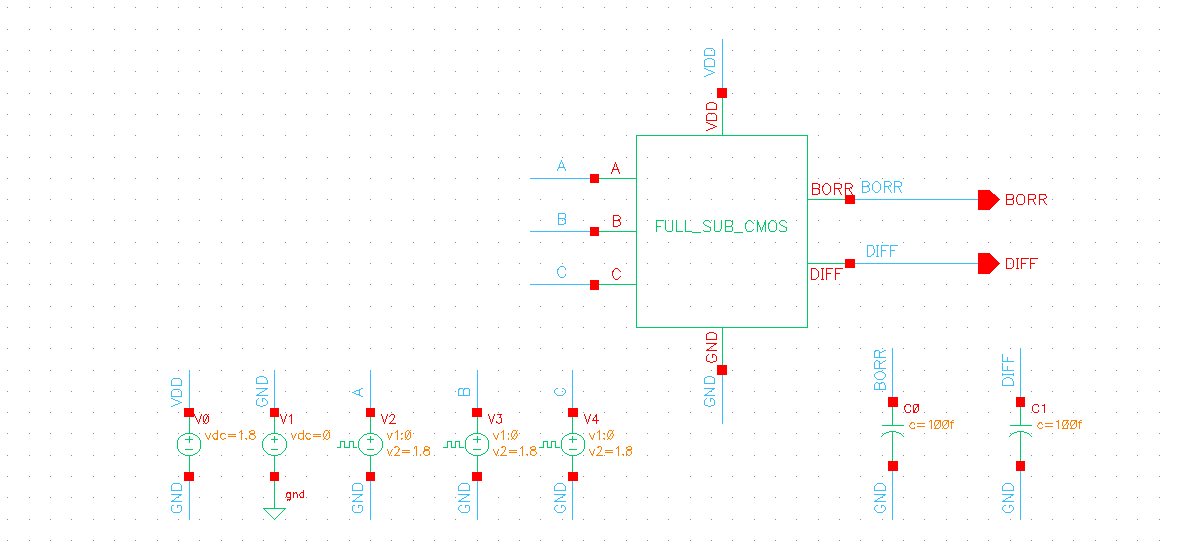
**Half SUBTRACTOR CMOS LOGIC:**

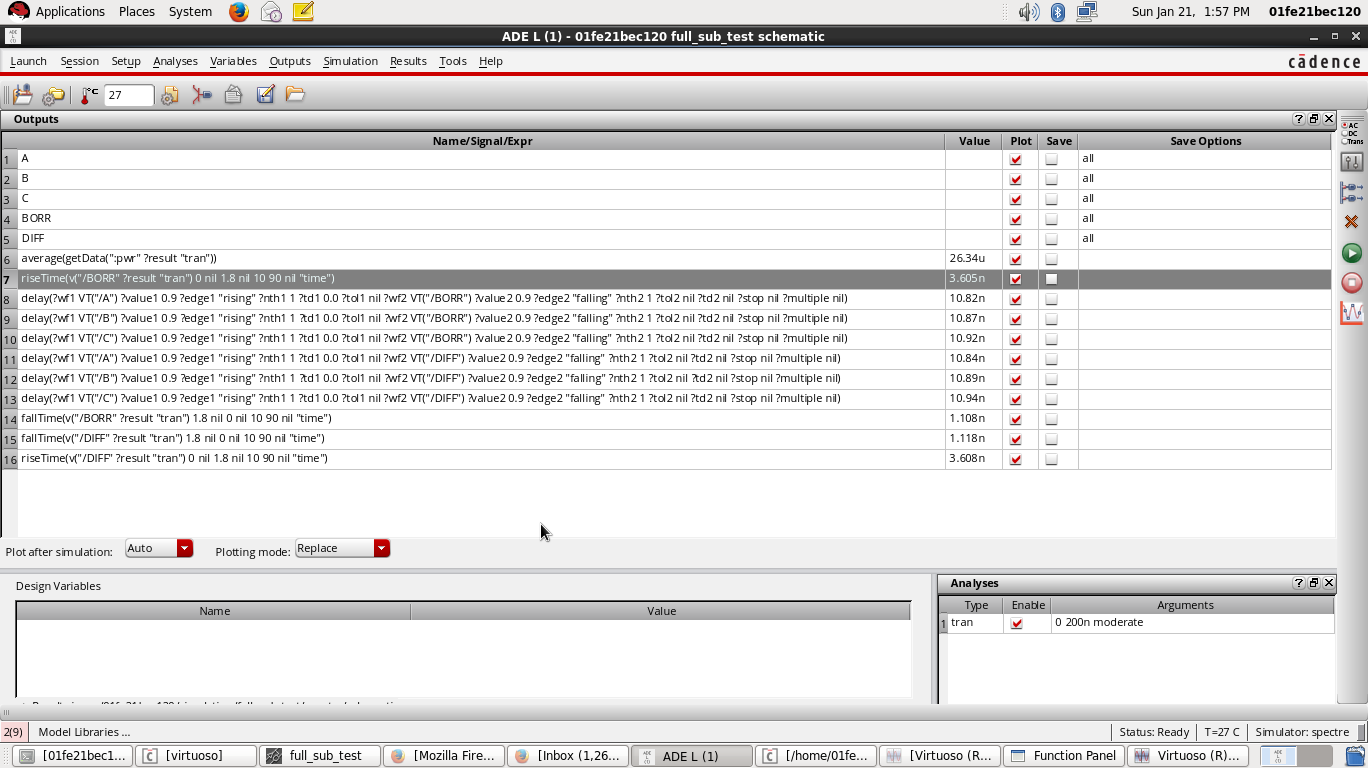
**Test schematic Half Subtractor CMOS logic:**

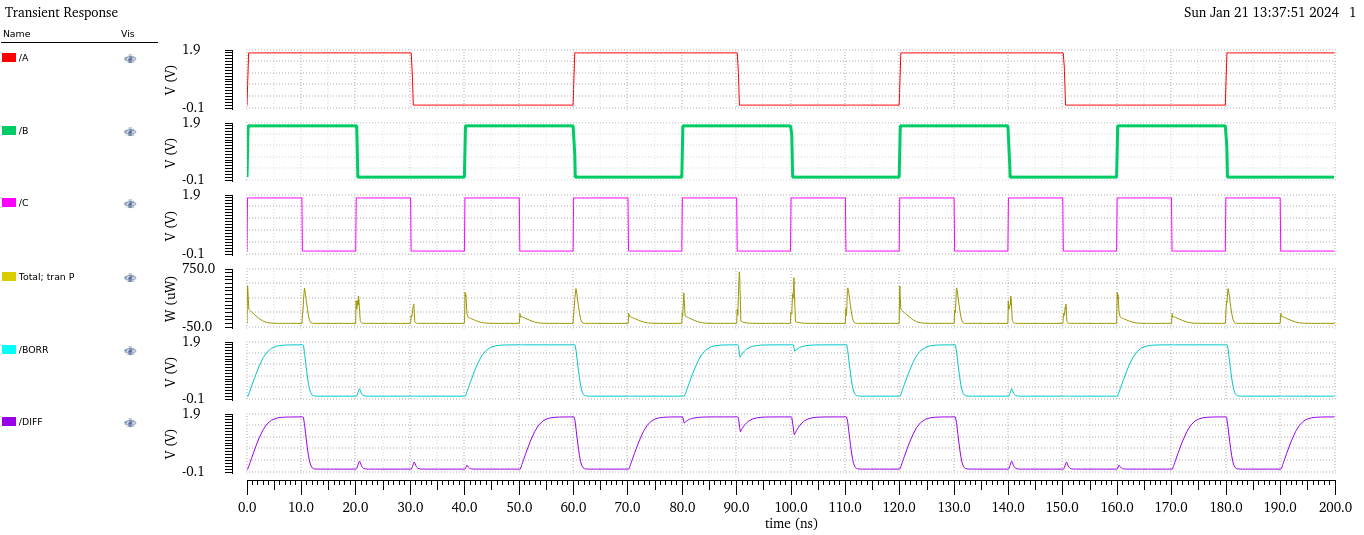


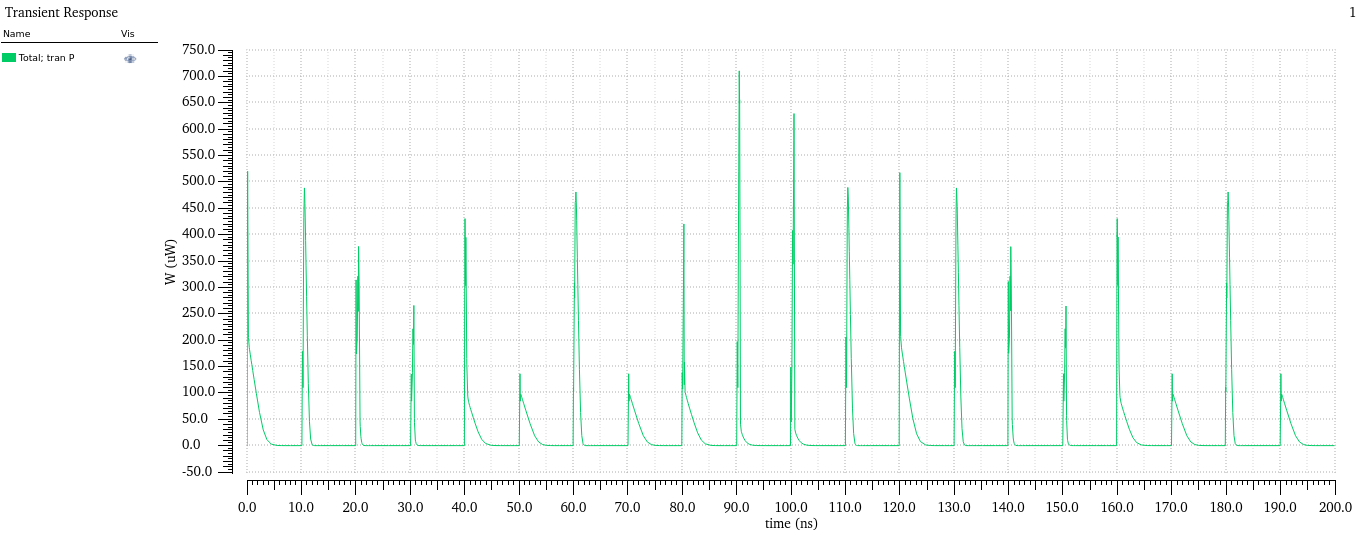
**Full Subtractor Schematic:**

**Full Schematic test schematic and Results:**

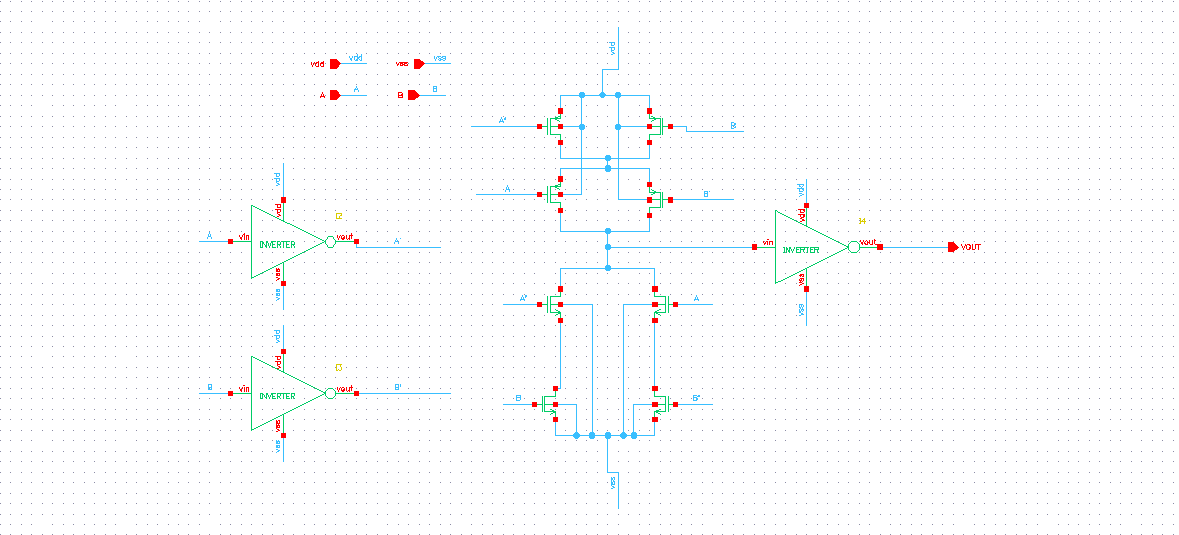




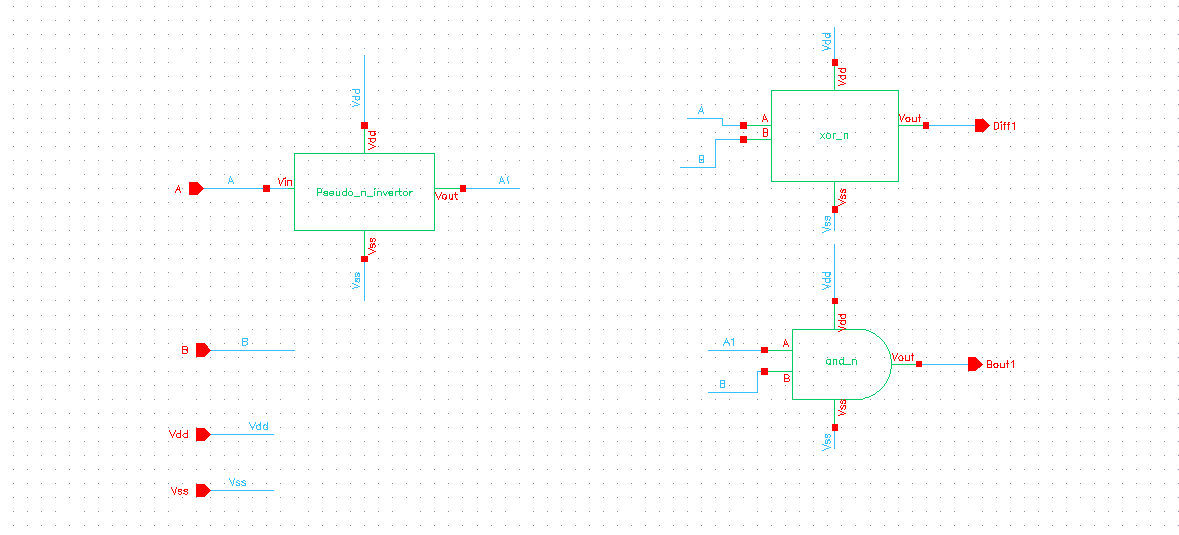


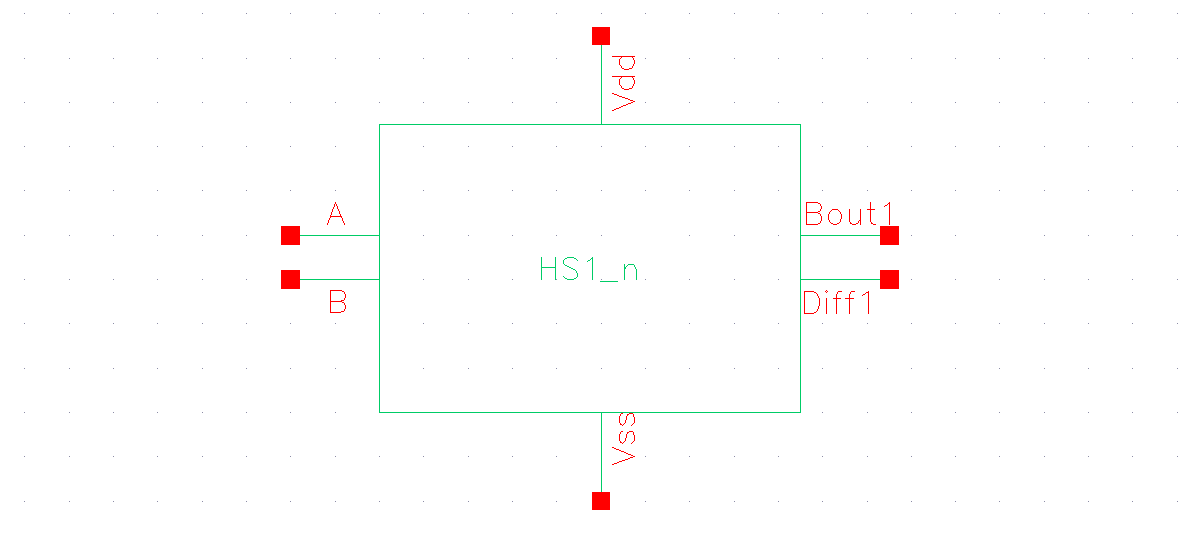


**Pseudo NMOS logic:**

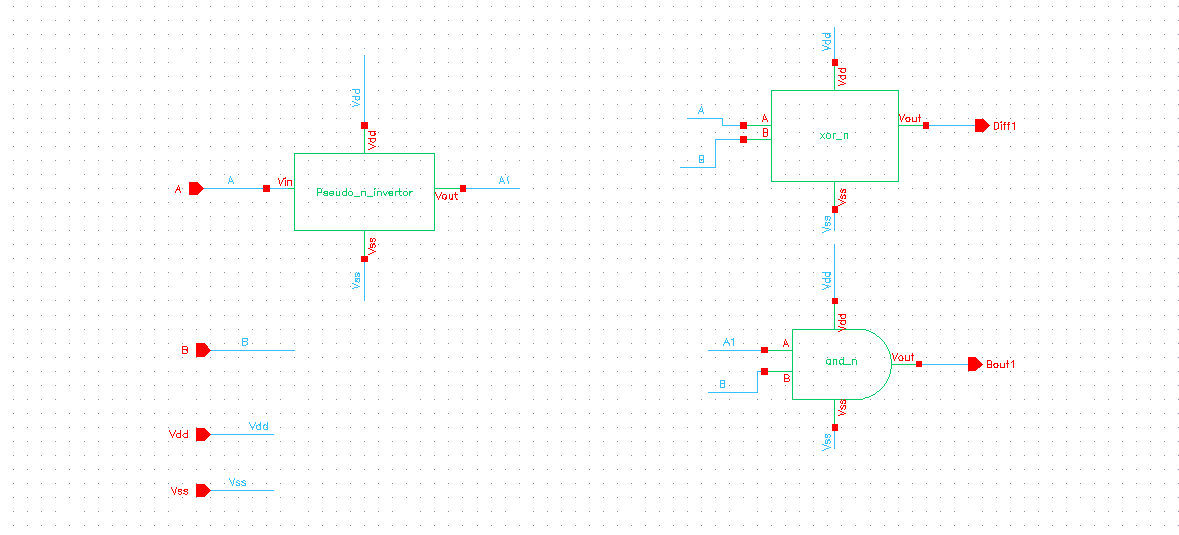
**Xor** **Schematic**:

**Pseudo Half Subtractror Schematic:**

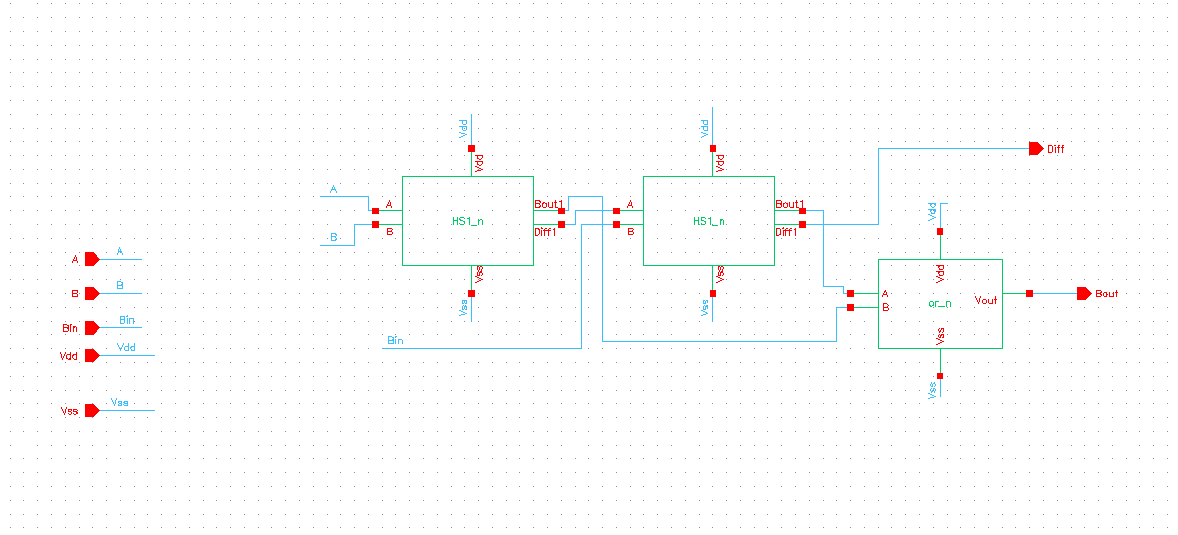


**Symbol**:

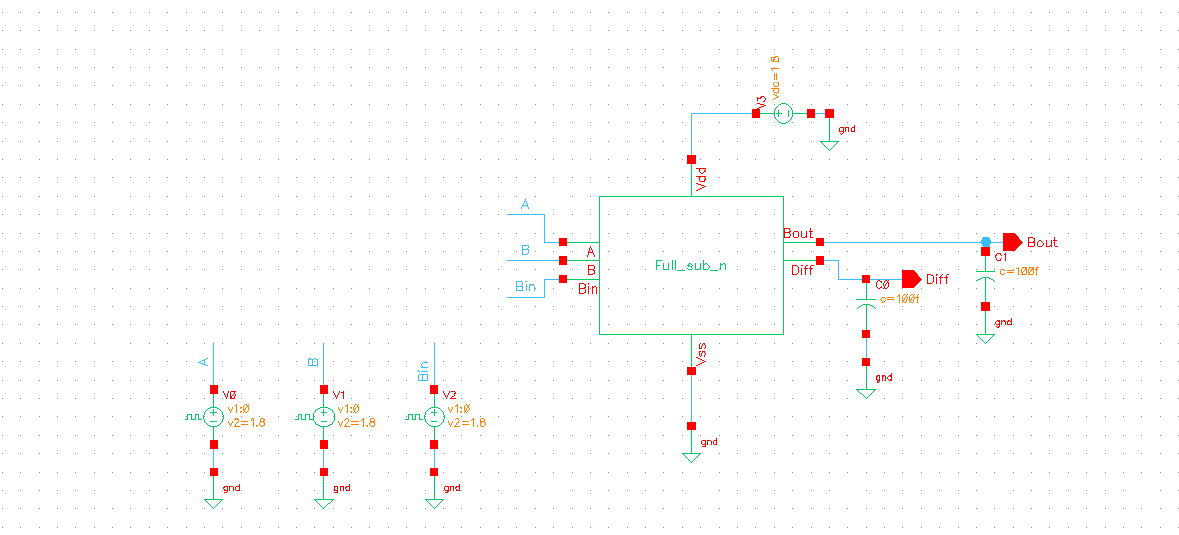
**Test Schematic:**

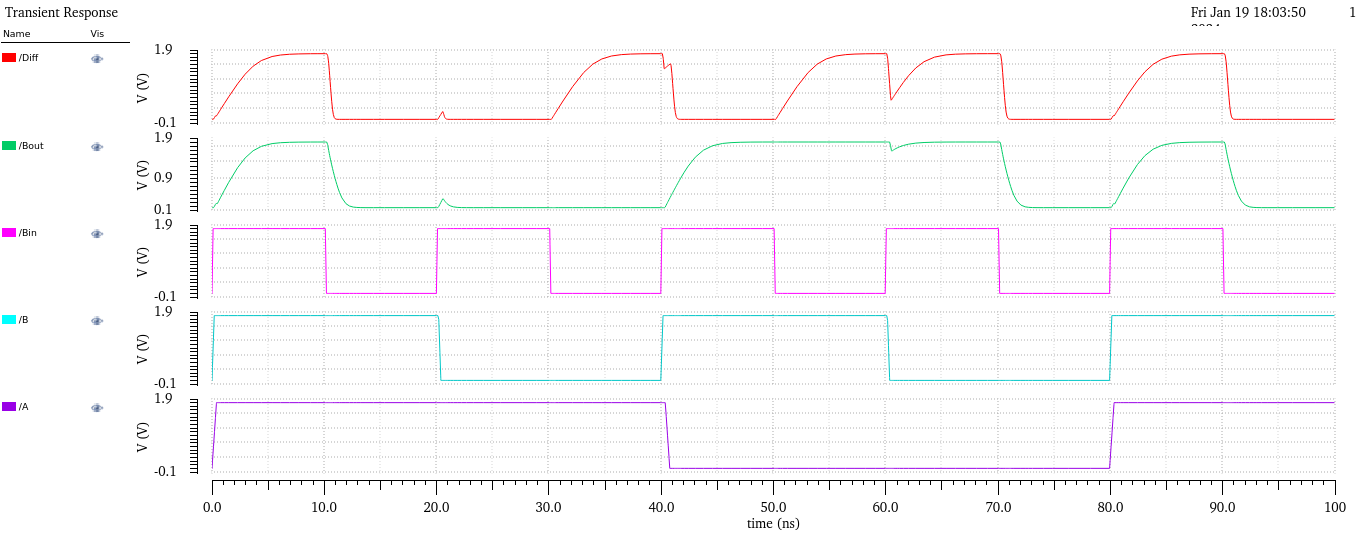


**Full Subtractor Schematic:**



**Full Subtractor Test Schematic and Result:**





**Results:**

|  |  |  |
| --- | --- | --- |
|  | **CMOS logic** | **Pseuodo Nmos logic** |
| **Rise time(Diff)** | 3.608ns | 3.9ns |
| **Fall time (Diff)** | 1.118ns | 421.4ps |
| **Rise time(Borrow)** | 3.605ns | 3.72ns |
| **Fall time(Borrow)** | 1.108ns | 2.12ns |
| **Power** | 26.34uW | 728uW |
| **Area** | 12n | 29n |

**Conclusion:**

In summary, Pseudo NMOS Logic outperforms CMOS Logic regarding speed (rise and fall times). CMOS Logic is more power-efficient, whereas Pseudo NMOS Logic consumes significantly more power.

CMOS Logic is generally favoured for its lower power consumption.

However, Pseudo NMOS Logic covers less area compared to CMOS Logic since the number of transistors used is comparatively less.